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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/541,881	07/07/2005	Wolfgang Stidl	DE03 0015 US	6245
65913	7590	01/25/2010	EXAMINER	
NXP, B.V. NXP INTELLECTUAL PROPERTY & LICENSING M/S41-SJ 1109 MCKAY DRIVE SAN JOSE, CA 95131			PEARSON, DAVID J	
			ART UNIT	PAPER NUMBER
			2437	
			NOTIFICATION DATE	DELIVERY MODE
			01/25/2010	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary

Application No.

10/541,881

Applicant(s)

STIDL ET AL.

Examiner

DAVID J. PEARSON

Art Unit

2437

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 December 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-9 and 13-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-9 and 13-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/GS/US)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

1. Claims 10-12 have been canceled. Claims 13-15 are newly added. Claims 1-9 and 13-15 have been examined.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/05/2009 has been entered.

Response to Arguments

3. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.
4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

5. Claims 1-6 and 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Force et al. (U.S. Patent 5,533,123; hereafter referred to as "Force"), and further in

view of Sutherland (U.S. Patent 6,292,898), Forward (U.S. Patent 4,376,269) and Little et al. (U.S. Patent Application Publication 2001/0011353; hereafter "Little").

For claim 1, Force teaches a microelectric circuit arrangement intended for protecting at least one electronic component against illicit manipulation and/or unauthorized access, having

At least one activating unit for checking that at least one activating condition is met (note column 23, lines 19-21) and for activating at least one preventing unit that is also associated with the circuit arrangement and that is connected to the activating unit (note column 23, lines 21-27), by means of which preventing unit the component can be at least partly de-activated and/or at least partly destroyed in the event of illicit manipulation and/or unauthorized access (note column 25, lines 14-34).

Force differs from the claimed invention in that they fail to teach:

Characterized in that the preventing unit is arranged

(j=4) to prevent the build-up of a high voltage and

(j=7) to switch on an increased current drain in the operating state of the quiescent state.

Sutherland teaches:

Characterized in that the preventing unit is arranged

(j=4) to prevent the build-up of a high voltage (note column 9, lines 41-49) and

(j=7) to switch on an increased current drain in the operating state of the quiescent state (note column 10, lines 4-9).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the checking unit of Force and the clamp to ground of Sutherland. One of ordinary skill in the art would have been motivated to combine Force and Sutherland because this active erasure of memory is much faster than passive erasure (note column 4, lines 14-26 of Sutherland).

The combination of Force and Sutherland differs from the claimed invention in that they fail to teach:

(j=1) to prevent an internal oscillator from beginning to oscillate.

Forward teaches:

(j=1) to prevent an internal oscillator from beginning to oscillate (note column 5, lines 62-67).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the combination of Force and Sutherland and the disabled oscillator of Forward. It would have been obvious to combine Force, Sutherland and Forward because combining prior art elements according to known methods would yield

the predictable results of disabling a circuit based a given condition (note column 5, lines 48-64 of Forward).

The combination of Force, Sutherland and Forward differs from the claimed invention in that they fail to teach:

(j=2) to prevent an oscillator for an external clock signal from beginning to oscillate.

Little teaches:

(j=2) to prevent an oscillator for an external clock signal (note paragraph [0185] from beginning to oscillate (note paragraph [0235]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the combination of Force, Sutherland and Forward and the disabled oscillator of Little. It would have been obvious to combine Force, Sutherland, Forward and Little because combining prior art elements according to known methods would yield the predictable results of disabling a circuit based a given condition (note paragraphs [0234]-[0235] of Little).

For claim 5, the combination of Force, Sutherland, Forward and Little teaches a method of protecting at least one electronic component against illicit manipulation and/or unauthorized access, characterized by the following method steps:

Checking that at least one activating condition is met by means of at least one activating unit (note column 23, lines 19-21 of Force),

In the event of illicit manipulation of the component and/or unauthorized access to the component activating at least one preventing unit that is connected to the activating unit (note column 23, lines 21-27 of Force) and

At least partly de-activating the operation of the component and/or at least partly destroying the component, by means of the preventing unit (note column 25, lines 14-34 of Force);

Characterized in that the at least partial de-activation of the operation of the component and/or the at least partial destruction of the component is carried out by

(j=1) preventing an internal oscillator from beginning to oscillate (note column 5, lines 62-67 of Forward).

(j=2) preventing an oscillator for an external clock signal from beginning to oscillate (note paragraph [0235] of Little).

(j=4) preventing the build-up of a high voltage (note column 9, lines 41-49 of Sutherland) and

(j=7) switching on an increased current drain in the operating state of the quiescent state (note column 10, lines 4-9 of Sutherland).

For claim 2, the combination of Force, Sutherland, Forward and Little teaches claim 1, characterized in that the preventing unit is constructed

In analog circuit technology or

In at least directly digital circuit technology, in the form of at least one fuse and/or at least one antifuse (note column 26, lines 16-20 of Force).

For claims 3 and 8, the combination of Force, Sutherland, Forward and Little teaches claims 1 and 5, characterized in that the activating unit is arranged

To recognize once or more than once at least one illicit command (note column 22, lines 15-18 of Force),

To recognize a multiplicity of difference illicit operations (note column 23, lines 46-52 of Force)

To issue at least one specific activating command (note column 25, lines 14-21 of Force)

To issue at least one activating command together with data that addresses a plurality of components by means of at least one group coding, or an individually coded component (note column 26, lines 45-67 of Force), and/or

To recognize once or more than once at least one physical attack on the component, by means of sensor circuitry belonging to the component that is intended for this purpose (note column 15, lines 42 and 64; column 16, line 13; column 17, line 36; column 18, line 51; column 19, line 55; column 21, line 28 of Force).

For claims 4 and 9, the combination of Force, Sutherland, Forward and Little teaches claims 1 and 5, characterized in that the preventing unit is arranged

(j=3) to switch off a high-voltage limiter, in particular by means of permanent programming,

(j=5) to reprogram the allocation of addresses and/or the allocation of data, and/or

(j=6) to load the memory element of the component with illicit values of data (note column 26, lines 16-21 of Force).

For claim 6, the combination of Force, Sutherland, Forward and Little teaches claim 5, characterized in the check on whether the activating condition is met is made

By analyzing at least one data stream applied from outside (note column 22, lines 15-18 of Force) or

By signals from the internal sensor circuitry of the component (note column 15, lines 42 and 64; column 16, line 13; column 17, line 36; column 18, line 51; column 19, line 55; column 21, line 28 of Force).

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Force, Sutherland, Forward and Little as applied to claim 5 above, and

further in view of Beuten et al. (U.S. Patent Application Publication 2003/0018902; hereafter referred to as "Beuten").

For claim 7, the combination of Force, Sutherland, Forward and Little differs from the claimed invention in that they fail to teach:

If the activation condition is met, recognition of this fact and the desired effects it is to have are placed in store in coded form in at least one memory element that is used for starting-up the component, and

The start-up, which initiates the appropriate actions, is repeated.

Beuten teaches:

If the activation condition is met, recognition of this fact and the desired effects it is to have are placed in store in coded form in at least one memory element that is used for starting-up the component (note paragraph [0014]), and

The start-up, which initiates the appropriate actions, is repeated (note paragraph [0014]).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the combination of Force, Sutherland, Forward and Little and the stored manipulation detection of Beuten. It would have been obvious to one ordinary skill in the art at the time of the invention to combine Force, Sutherland, Forward, Little

and Beuten because it would permit an orderly power down of the system without any loss of data.

7. Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Force, Sutherland, Forward, Little and Beuten as applied to claim 7 above, and further in view of McCurdy et al. (U.S. Patent 5,117,222; hereafter "McCurdy").

For claim 13, the combination of Force, Sutherland, Forward, Little and Beuten teaches a method of protecting at least one electronic component against illicit manipulation and/or unauthorized access, characterized by the following method steps:

Checking that at least one activating condition is met by means of at least one activating unit (note column 23, lines 19-21 of Force),

If at least one activation condition is met, recognition of this fact and the desired effects it is to have are placed in store in coded form in at least one memory element that is used for starting-up the component (note paragraph [0014] of Beuten), and

At the next attempt to start up the product (note paragraph [0014] of Beuten);

Reading out the activation condition (note paragraph [0014] of Beuten); and

At least partly de-activating the operation of the electronic component and/or at least partly destroying the electronic component, by means of the preventing unit (note column 25, lines 14-34 of Force);

Characterized in that the at least partial de-activation of the operation of the component and/or the at least partial destruction of the component is carried out by;

switching on an increased current drain (note column 10, lines 4-9 of Sutherland);

Blocking generation of high voltage (note column 9, lines 41-49 of Sutherland);

Stopping an internal clock signal (note column 5, lines 62-67 of Forward).

The combination of Force, Sutherland, Forward, Little and Beuten differs from the claimed invention in that they fail to teach:

Ignoring an external clock signal.

McCurdy teaches:

Ignoring an external clock signal (note column 3, lines 60-65).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the combination of Force, Sutherland, Forward, Little and Beuten and the ignored clock signal of McCurdy. It would have been obvious to combine Force, Sutherland, Forward, Little, Beuten and McCurdy because combining prior art elements according to known methods would yield the predictable results of disabling a circuit based a given condition (note column 3, lines 55-65 of McCurdy).

For claim 14, the combination of Force, Sutherland, Forward, Little, Beuten and McCurdy teaches claim 13, characterized in the check on whether the activating condition is met is made

By analyzing at least one data stream applied from outside (note column 22, lines 15-18 of Force) or

By signals from the internal sensor circuitry of the component (note column 15, lines 42 and 64; column 16, line 13; column 17, line 36; column 18, line 51; column 19, line 55; column 21, line 28 of Force).

For claim 15, the combination of Force, Sutherland, Forward, Little, Beuten and McCurdy teaches claim 13, characterized in that the activation takes place

(i=1) as a result of the recognition once or more than once of at least one illicit command (note column 22, lines 15-18 of Force),

(i=2) as a result of the recognition of a multiplicity of difference illicit operations (note column 23, lines 46-52 of Force)

(i=3) as a result of the issue of at least one specific activating command (note column 25, lines 14-21 of Force)

(i=4) as a result of the issue of at least one activating command together with data that addresses a plurality of components by means of at least one group coding, or an individually coded component (note column 26, lines 45-67 of Force), and/or

(i=5) as a result of the recognition once or more than once of at least one physical attack on the component, by means of sensor circuitry belonging to the

component that is intended for this purpose (note column 15, lines 42 and 64; column 16, line 13; column 17, line 36; column 18, line 51; column 19, line 55; column 21, line 28 of Force).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Foster et al. (U.S. Patent Application Publication 2003/0200453) teaches a clock can be stopped upon a tamper detection (note paragraph [0056]).

Krishnaiyer et al. (U.S. Patent 4,023,163) teaches preventing clock pulses from being transmitted upon a reset signal (note column 11, lines 3-8)

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DAVID J. PEARSON whose telephone number is (571)272-0711. The examiner can normally be reached on Monday - Friday, 7:30am - 5:00pm; off every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Emmanuel Moise can be reached on (571) 272-3865. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David J Pearson/
Examiner, Art Unit 2437